Speci cation OPB-SPI Slave

Contents

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1.2 3imitatiSPI 0 GETq149 0 1 148.8.29501.92 cm[]0 d 0 J 0.398 w49 0 m 3.273 0 l SQ 20.662 G 0 590

1 Introduction

This document describe a SPI Slave core designed for the Xilinx EDK. [?]

1.1 Features

4 Registers

4.1 Adressmap

Name	Adress	Acess	Description
SPI_CR	0x00	R/W	SPI Control Register
SPI_SR	0x04	R/W	SPI Status Register
SPI_TD	0x08	W	SPI Transmit Data Register
SPI_RD			

4.3 SPI_SR

Bit	Name	Acess	Reset Value	Description
31	TX Prog Full	R	0	Prog Full Flag 1: FIFO Prog Full

This Register is only available if C

4.10 RX_

Bit	Name	Acess	Reset Value	Description
31	TX			

5 System Integration

To integrate this IP-Core in your System, unzip the opb

```
#define XSS_DGIE_Bit_Enable 0x0001

// Interrupt /Enable Status Register
#define XSS_ISR_Bit_TX_Prog_Empty  0x0001
#define XSS_ISR_Bit_TX_Empty       0x0002
#define XSS_ISR_Bit_TX_Underflow   0x0004
#define XSS_ISR_Bit_RX_Prog_Full   0x0008
#define XSS_ISR_Bit_RX_Full        0x0010
#define XSS_ISR_Bit_RX_Overflow    0x0020
#define XSS_ISR_Bit_SS_Fall        0x0040
#define XSS_ISR_Bit_SS_Rise        0x0080
#define XSS_ISR_Bit_TX_DMA_done 0x0100
#define XSS_ISR_Bit_RX_DMA_done 0x0200

// TX DMA Control Register
#define XSS_TX_DMA_CTL_EN 0x0001

// RX DMA Control Register
#define XSS_RX_DMA_CTL_EN 0x0001
```

6 Operations

7 Architecture