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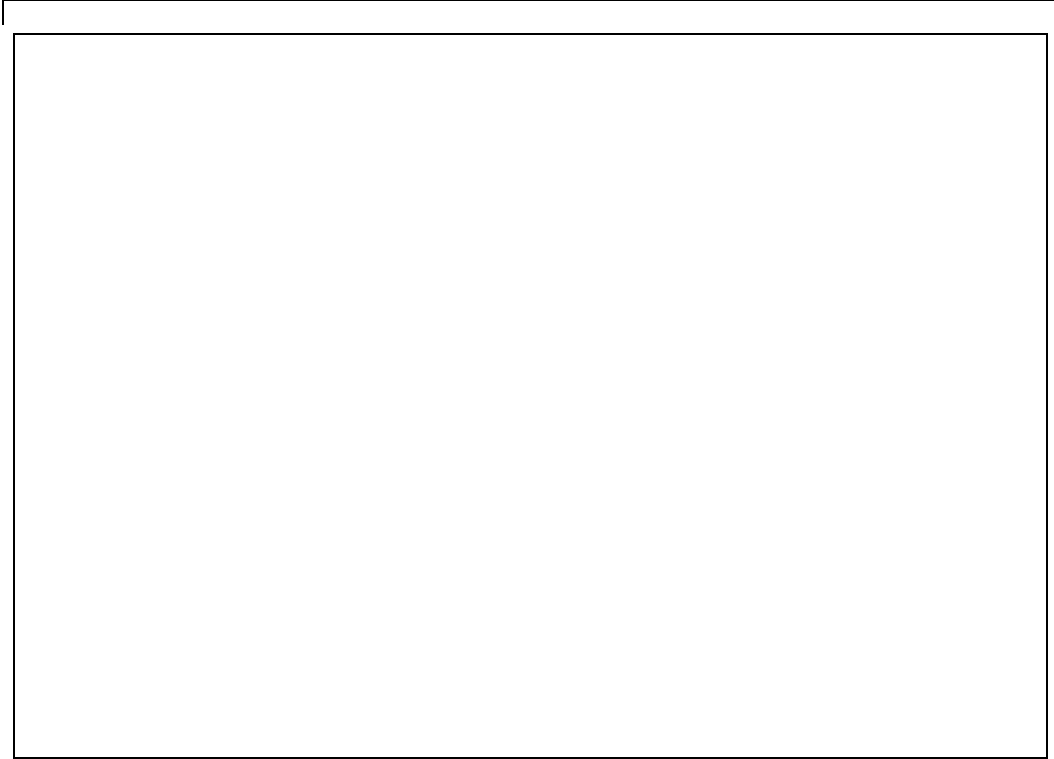
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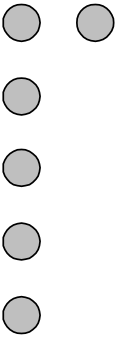
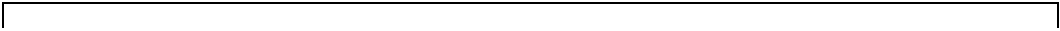
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PRELIMINARY



2.0 PRINCIPLES OF OPERATION

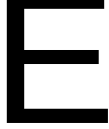
The 3 Volt FlashFile memories include an on-chip WSM to manage block erase, program, and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure, program, and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep

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When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

Table 6. Status Register Definition

WSMS	ESS	ECLBS	PSLBS	VPPS	PSS	DPS	R
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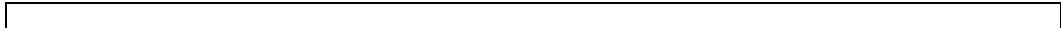
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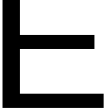


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6.0 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Temperature under Bias.....	–10 °C to +80 °C
Storage Temperature	–65 °C to +125 °C
Voltage On Any Pin (except V _{PP} , and RP#).....	–2.0 V to +7.0 V ⁽²⁾
V _{PP} Voltage	–2.0 V to +14.0 V ^(1,2)
RP# Voltage	–2.0 V to +14.0 V ^(1,2,4)
Output Short Circuit Current	100 mA ⁽³⁾



6.4 DC Characteristics—Commercial Temperature

	2.7 V V _{CC}	3.3 V V _{CC}	Test
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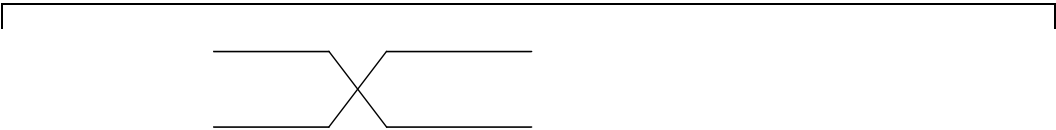


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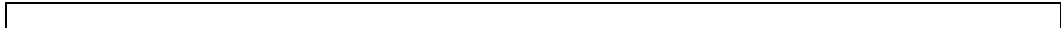
PRELIMINARY TEST POINTS INPUT

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