Memory Controller IP Core

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Revision History

Rev.	Date	Author	Description
0.1	7/4/01	Rudolf Usselmann	First Draft
0.2	9/4/01	RU	- Added timing diagrams and descriptions. - Modified CSC and TMS registers. - Added IOs for SSRAMS and external masters.
0.3	19/4/01	RU	- Updated core architecture overview drawing. - Fixed several minor syntax errors. - Renamed CSC_MASK to BA_MASK register. - Added Power Down Mode section. - Added External Bus Master Section.
0.4	29/4/01	RU	- Added Bandwidth Section. - Added Table to Power-On Configuration Section. - Added POC register Output - Added Appendix C: IO Buffers - Added Appendix D: Wiring Examples. - Added SSRAM Timing diagrams. - Filled in Memory Organization Section. - Filed in Synchronous Chip Select Devices Section. - Filled in Appendix A: HW Configuration.
1.0	13/5/01	RU	- Added dynamic bus sizing section - Moved Refresh Prescaler and Refresh Early from HW Configuration section in to CSR register. - Added RMW cycle section. - Added Error Signaling Section.
1.1	30/5/01	RU	- Added Section 2.5 Clocks. - Fixed IO names to match the core. - Added WISHBONE Clock and Reset signals.
1.2	25/6/01	RU	- Cleaned up document for references to SRAM and SSRAM. - Add TSM Register specification for SSRAM.

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Introduction

This is a universal Memory Controller core. It supports a variety of memory

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2.1. WISHBONE Interface

The Memory Controller core includes a WISHBONE host interface.This interface is WISHBONE SoC bus specification Rev. B compliant. This implementation implements a 32 bit bus width and does not support othISH09NE w.ntati(-)]TJ1.91.8 -4.26.5 Tm[

Figure 2: Keep Row Open Initial SDRAM Access

The second mode, is to close the row immediately after the Read or Write operation. Here, each new access has to execute the Activate command before performing the Read or Write operation. This will help systems that are known to fetch

The table below illustrates sample settings for various SDRAM speeds and bus frequencies. Actual values may vary. Please check the SDRAM data sheet for details.

The figure above illustrates a Asynchronous Chip Select Device write cycle. The memory Controller core will assert the address, data, chip select and write enable at the same time. After Twpw nS, it will de-assert write enable. After Twd nS it will de-assert the address, data and chip select. The next write will not be performed until Twwd nS have elapsed.

The actual internal write operation of a attached Flash might take much longer

Figure 10: Synchronous Chip Select Devices Read Cycle

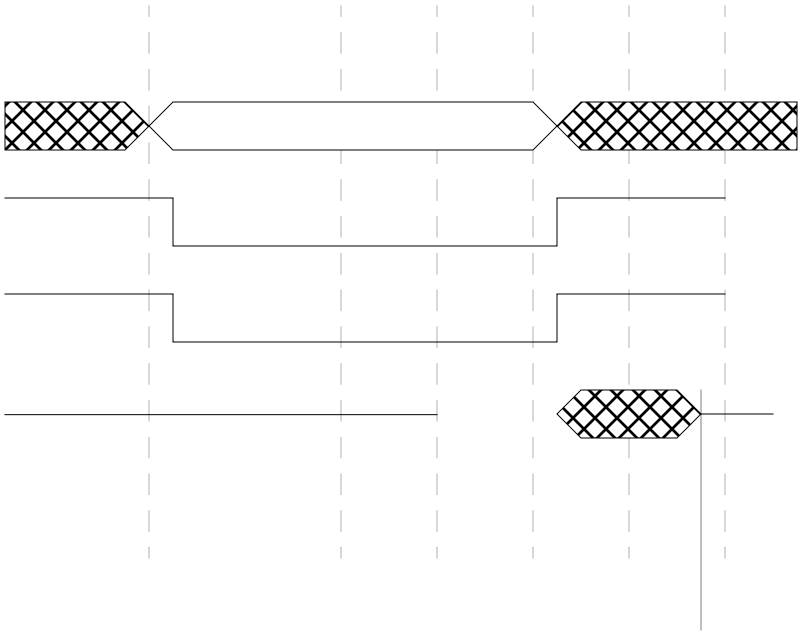


Figure 11: Synchronous Chip Select Devices Write Cycle

vide larger rows sizes (e.g. 8 bit wide SDRAM devices) or by extending the row

Figure 15: Power Down Mode Enter/Resume

The susp_req signal must be de-asserted, once suspended output is activated. The resume_req input may be asserted at any time (even with susp_req). The Memory Controller will sample resume_req only once it has entered suspended state (suspended output active).

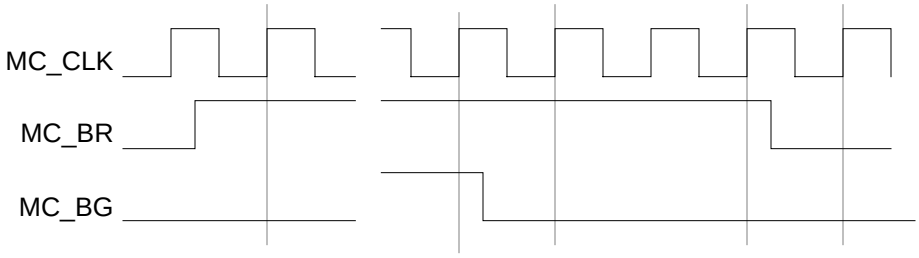
Before entering suspended state, the Memory Controller will place all attached SDRAMs in to “Self Refresh” mode. In this mode the SDRAMs consume very little power, do not require an external clock, and maintain memory contents by performing internal refresh cycles.

3.11.Memory Bus Arbitration

The Memory Controller includes and Arbiter for External Bus Masters. External Bus masters may acquire the bus by asserting mc_br. Once grant has been given (mc_gnt asserted) the external bus master may use the memory bus. External bus masters must keep the mc_br signal asserted for the entire duration they are on

If the memory controller de-asserted mc_gnt before the external master releases mc_br, this indicates to the external bus master to get of the bus as soon as possible, and indicate that by de-asserting mc_br.

Figure 17: Memory Controller Requests Bus back



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Core Registers

This section describes all control and status registers

Value after reset:
CSR: 0000h

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Core IOs

5.1. Interface IOs

The SoC interface is WISHBONE Rev B compliant.

Table 11: Host Interface (WISHBONE)

Name	Width	Direction	Description
CLK	1	I	WISHBONE Clock Input
RST	1	I	WISHBONE Reset Input The reset is asynchronous and an active low signal.
WB_ADDR_I	32	I	Address Input
WB_DATA_I	32	I	Data Input
WB_DATA_O	32	O	Data Output
WB_SEL_I	4	I	Indicates which bytes are valid on the data bus.
WB_WE_I	1	I	Input for slave. Indicates a Write Cycle when asserted high.
WB_CYC_I	1	I	Input for slave. Encapsulates a valid transfer cycle.
WB_STB_I	1	I	Input for slave. Indicates a valid transfer.
WB_ACK_O	1	O	Acknowledgment Output. Indicates a normal Cycle termination.
WB_ERR_O	1	O	Error acknowledgment output. Indicates an abnormal cycle termination.

Table 13: Memory Interface IOs

Name	Width	Direction	DescriptionFl7j 3 n -7119 22no3a7lJ -7119 4(Fl7j 3
MC_CAS_	1	O	Memory Column Address Select
MC_RAS_	1	O	memory Row Address Select
MC_CKE_	1	O	Memory Clock Enable
MC_CS_	8	O	Memory Chip Select Outputs
MC_RP_	1	O	Flash Reset/Power-Down
MC_STS	1	I	Flash Ready/Busy Status
MC_VPEN	1	O	Flash Erase/Program enable
MC_ADSC_	1	O	SSRAM ADSC signal
MC_ADV_	1	O	SSRAM Address Advance
MC_ZZ	1	O	SSRAM Snooze Enable

Total IOs (after inserting Bi-Dir buffers for Data Lines): 87

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Appendix A

Core HW Configuration

This Appendix describes the configuration of the core. This step is performed before final Synthesis and tape-out of the core.

A.1. Address Space Selection

The Memory Controller includes configuration registers and memory address spaces. The address range for each of them can be individual selected by editing

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Appendix D

Wiring Examples

This Section demonstrates how to connect various Memory Devices to the Memory Controller. This are just examples, and actual connections might vary. Specifically which chip select is used, is entirely up to the system designer.

Figure 20: Connecting FLASH Memories

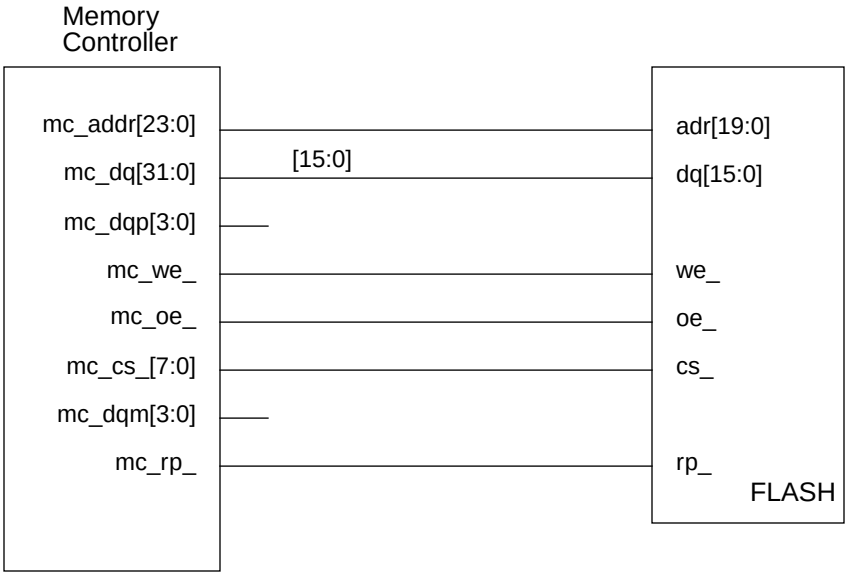
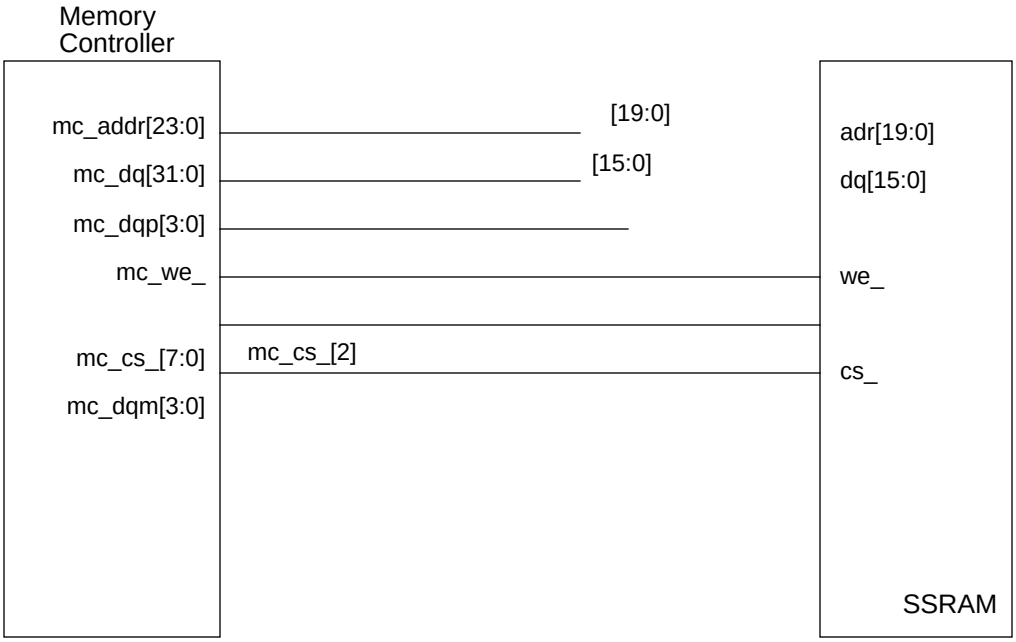
Figure 23: Connecting (x16) SSRAM Memories