1. Introduction

The floating point unit (FPU) implemented duri

The number represented by the single-precision format is:

3.2 Exceptions

3.2.4 Underflow

Two events cause the underflo

The standard specifies four rounding modes:

3.3.1 Round to nearest even

This is the standard default rounding. The value is rounded up or down to the nearest infinitely precise result. If the value is exactly halfway between two infinitely precise results, then it should be rounded up to the nearest infinitely precise even.

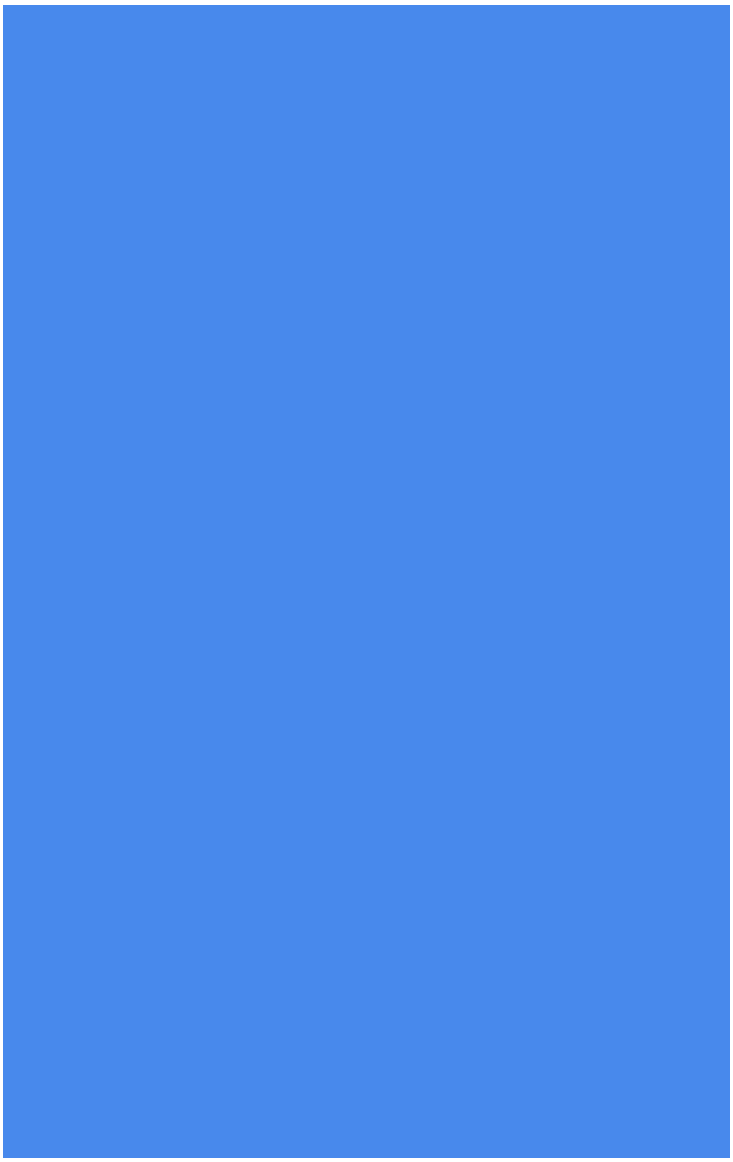
For example:

Unrounded	RC	*P*

Step 1: multiply fractions and calculate the result exponent.

$$\begin{array}{rl} & 1.1001 \\ \times & 1.0010 \\ \hline & 1.11000010 \end{array}$$

4.3 Division



The division was done serially using t1 Tbasic al

4.2 Compilation and Synthesis

The FPU core was compiled and synthesized successfully with *Altera Quartus II v.5* and *Synplify Pro 8.1*. The *Cyclone I–EP1C6Q240C6* was the intended FPGA.

6. References

1. IEEE computer society: IEEE Standard 754 for Binary Floating-Point Arithmetic, 1985.