VDK9 R ½

Design document – Version 1.00 – June 12th 2001

Control Unit

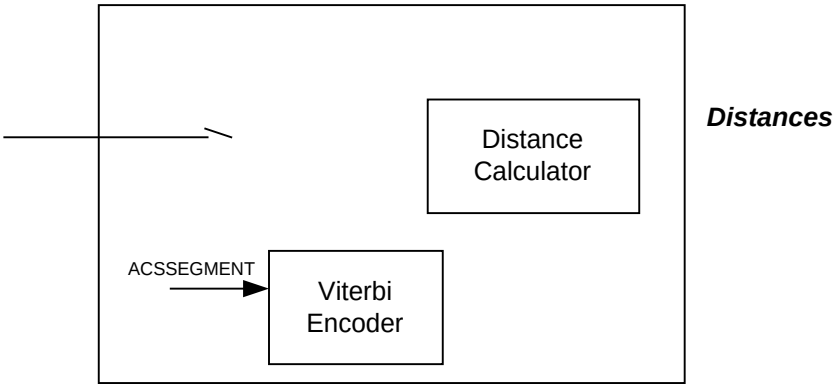
Control Unit is used to provide control signals for the other components. Those signals are listed on Table I.

Table I. Control Unit Signals

Signal Name	Description
`Clock1` and `Clock2`	`Clock1` and Clock2 are signals with frequency equals to ¼ of `Clock` frequency.

BMG (Branch Metric Generator) Unit

BMG Unit block diagram is shown on Figure 2.



The Modified Comparison Rule processor uses two 2’s-complement adders and two XOR gate to work.

Note that there is an Enable signal on the comparator. This signal is come from the Control Unit.

Anyway, should we use standard RAM operations the RAM Interface job is to do the following process :

- Select which block of RAM used to read the metric and which one is used to write the metrics we've just calculated. (On the source code, `MMBlockSelect` signal do this).
- Upon `RESET`, the values of metrics on both block of RAM have to be set to 0.
- The update process on the ACS processor happened on every rising edge of `Clock1`

Let’s take a simple example using a K=2 convolutional code case. Suppose that on level *t*

The write operation on the survivor memory will occur every 2 falling edge of `Clock1`. Remember that the number of ACS is only 4, while the Data Bus is 8 bit wide.

The read operation will occur on every rising edge of Clock1.

The survivor memory timing diagram is shown on Figure 11.

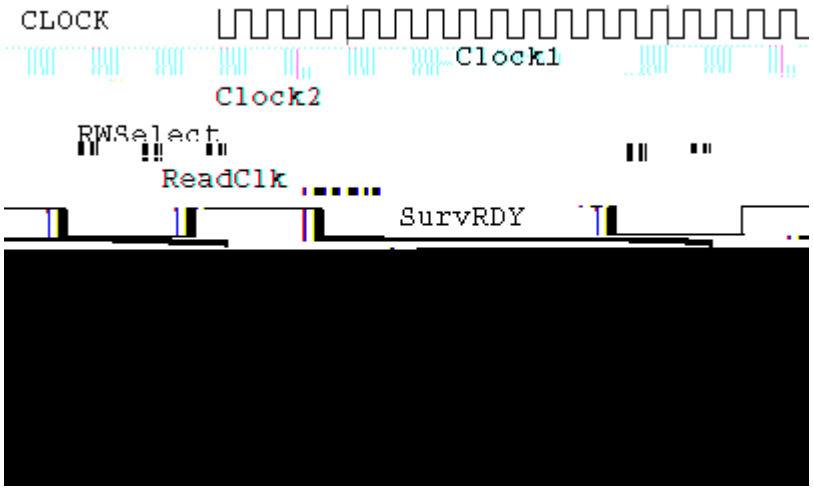
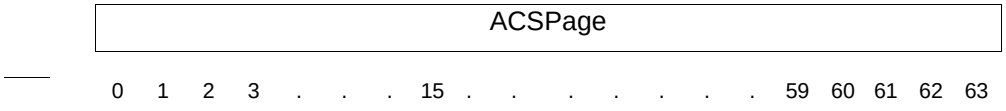


Figure 11. Survivor Memory Timing Diagram

The Survivor Memory Addressing Scheme

Write Operation

The address for write operation is assembled from the combination of the value of ACSPage [5:0] and the value of ACSSegment [5:1].



Read Operation

For read operation, the address is assembled from the `TBPage` signal from the MMU, and `AddressTB` signal coming from the Traceback Unit.