Here, one of the interfaces of the DUT, is now connected to another IP Core. Now most likely the BFM and associated library routines must be rewritten to provide the same functionality as in the module level test bench. After the BFM has been adjusted to the new interface, and the DUT instance has been updates, the entire test bench can be reused.

In this case, the Verilog Top Level, instantiates the DUT and a VERA top level. The VERA top level instantiates the BFMs, library and test cases.

Figure 5: Multi Language Test Bench

3.1. Reusability Guidelines

Her are some pointers that should help in designing a test bench that can be easily reused.

- Partition the Test Bench
  Divide the test bench in to logically distinguished blocks:
  - Startup Section

- POR & Clock section
  In this section all clocks and power on reset sequences are -.210 .l81.3333 T41

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4

BFMs

Bus Functional Models (BFMs) create the iterface between a DUT and the test bench. The main prupose is to hide interface specific transaction and provide a low level generic task interface. This low level interface must be extreamly flexible and